Response to the Rejection based on Double Patenting

Claims 1-3, 5-8, 10-13, 15-18, and 20-28 were rejected under the judicially created doctrine of double patenting over Claims 1-17 of co-owned U.S. Patent No. 5,973,378. Applicants amend the claims herein to provide patentable distinctiveness from the claims of the '378 patent, and therefore respectfully requests allowance of all claims.

Response to the Claim Rejections Under 35 U.S.C §§ 102 and 103

Claims 1-3, 5-8, 10-13, 15-18, and 20-28 are rejected under 35 U.S.C. § 102(b) as being anticipated by either U.S. Patent No. 5,430,320 issued to Lee, et al. or Japanese Patent No. 06-250214 issued to Tanenaka. The rejection asserts that either Lee or Tanenaka allegedly teaches each element of the claims. Claims 1-3, 5-8, 10-13, 15-18, and 20-28 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Tanenaka in view of Lee. The rejection asserts that Tanenaka allegedly teaches each element of the claims except for gate oxide sidewalls including the same metal as the gate electrode for ease of processing and design improvement, which is allegedly taught by Lee.

The present invention is directed toward a semiconductor device comprising a gate electrode formed of a first metal later and a second metal layer on the first metal layer. Both of the metal layers are anodized after laminating.

A width of the first metal layer is narrower than that of the second metal layer because the anodization rate of the first metal layer is greater than the anodization rate of the second metal layer. Thus, it is possible to weaken an electric field around the drain of the semiconductor device.

None of the cited art teaches or suggests the width of the first metal layer being narrower than the width of the second metal layer. Further, none of the cited art suggests having anodization rates differ between the metal layers.

In view of the foregoing distinctions, Applicants respectfully submit that independent Claims 1, 6, 11, 16, 21, and 25 are patentably distinguished over the cited art. Applicants respectfully submit that Claims 1, 6, 11, 16, 21, and 25 are in condition for allowance, and Applicants respectfully request allowance of Claims 1, 6, 11, 16, 21, and 25.

Claims 2-3, 7-8, 12-13, 15, 17-18, 20, 22-23, 26-27 and new Claims 29-38 depend either directly or indirectly from one of the independent claims. Each dependent claim further defines the independent claim from which it depends. In view of the foregoing remarks regarding Claims 1, 6, 11, 16, 21, and 25, Applicants respectfully submit that Claims 2-3, 7-8, 12-13, 15, 17-18, 20, 22-23, 26-27 and new Claims 29-38 are likewise in condition for allowance. Applicants respectfully request

allowance of dependent Claims 2-3, 7-8, 12-13, 15, 17-18, 20, 22-23, 26-27 and new Claims 29-38.

Summary

In view of the above amendments and remarks, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 5/21/01

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VERSION TO SHOW CHANGES MADE

In the Claims:

Claims 5, 10, 24, and 28 have been canceled.

New claims 29-38 have been added.

Claims 1, 6, 11, 16, 21, and 25 have been amended as follows.

1. (Amended) A semiconductor device comprising:

a semiconductor layer [having at least] comprising a source region, a drain region, and a channel region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a first conductive layer formed on said gate insulating film wherein said first conductive layer extends over said channel region; [and]

a second conductive layer formed on said first conductive layer[,] ; and

an insulating film comprising anodization oxide of said first and second conductive layers,

[wherein said first conductive layer comprises tantalum and said second layer comprises aluminum, and

wherein said first conductive layer is thinner than said second conductive layer]

wherein each of said first and second conductive layers comprises a material selected from the group consisting of

molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt,

wherein an anodization rate of said first conductive layer is greater than that of said second layer so that a width of said first conductive layer is narrower than that of said second conductive layer, and

wherein said insulating film is formed on at least side surfaces of said first and second conductive layers.

6. (Amended) A semiconductor device comprising:

a semiconductor layer [having at least] comprising a source region, a drain region, and a channel region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a first conductive layer formed on said gate insulating film wherein said first conductive layer extends over said channel region; [and]

a second conductive layer formed on said first conductive layer [wherein said first conductive layer comprises a different material from said first conductive layer,] ; and

an insulating film comprising anodization oxide of said first and second conductive layers,

wherein each of said first and second conductive layers comprises a material selected from the group consisting of

molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt, [and

wherein said first conductive layer is thinner than said second conductive layer]

wherein an anodization rate of said first conductive layer is greater than that of said second layer so that a width of said first conductive layer is narrower than that of said second conductive layer, and

wherein said insulating film is formed on side surfaces of said first and second conductive layers and a top surface of said second conductive layer.

11. (Amended) A semiconductor device comprising:

a semiconductor layer [having at least a channel region formed on an insulating surface];

a gate insulating film formed on said semiconductor layer;

a first conductive layer formed on said gate insulating film wherein said first conductive layer extends over said channel region; [and]

a second conductive layer electrically connected to said first conductive layer[,] ; and

an insulating film comprising oxide of said first and second conductive layers,

[wherein said first conductive layer comprises tantalum and said second layer comprises aluminum, and

wherein said first conductive layer is thinner than said second conductive layer]

wherein each of said first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt,

wherein a width of said first conductive layer is narrower than that of said second conductive layer, and

wherein said insulating film is formed on at least side surfaces of said first and second conductive layers.

16. (Amended) A semiconductor device comprising:

a semiconductor layer [having at least a channel region formed on an insulating surface];

a gate insulating film formed on said semiconductor layer;

a first conductive layer formed on said gate insulating film wherein said first conductive layer extends over said channel region; [and]

a second conductive layer electrically connected to said first conductive layer wherein said first conductive layer comprises a different material from said first conductive layer[,] ; and

an insulating film comprising oxide of said first and second conductive layers,

wherein each of said first and second conductive layers comprises a material selected from the group consisting of molybdenum, tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt, [and

wherein said first conductive layer is thinner than said second conductive layer]

wherein a width of said first conductive layer is narrower than that of said second conductive layer, and

wherein said insulating film is formed on side surfaces of said first and second conductive layers and a top surface of said second conductive layer.

21. (Amended) A semiconductor device comprising:

a gate electrode comprising a first conductive layer formed on an insulating surface and a second conductive layer formed on said first conductive layer;

an insulating film formed on said gate electrode;

a semiconductor layer [having at least] comprising a source region, a drain region, and a channel region formed on said insulating film,

wherein said first layer and said second layer comprises a material selected from the group consisting of molybdenum,

tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt, and

[wherein said first layer is thinner than said second layer]

wherein a width of said second conductive layer is narrower than that of said first conductive layer.

25. (Amended) A semiconductor device comprising:

a gate electrode comprising a first conductive layer formed on an insulating surface and a second conductive layer formed on said first conductive layer;

[an] a gate insulating film formed on said gate electrode;

a semiconductor layer [having at least] comprising a source region, a drain region, and a channel region formed on said insulating film, and

[an oxide film formed on at least side surfaces of said gate electrode, said oxide film comprises an oxide of a material of said gate electrode,]

an insulating film comprising oxide of said first and second conductive layers,

wherein said first layer and said second layer comprises a material selected from the group consisting of molybdenum,

tantalum, aluminum, chromium, nickel, zirconium, titanium, palladium, silver, copper, and cobalt, and

[wherein said first layer is thinner than said second layer]

wherein a width of said second conductive layer is narrower than that of said first conductive layer, and

wherein said insulating film is formed on at least side surfaces of said first and second conductive layers.